1. Front end specifications - preliminary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Nominal value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMT gain</td>
<td>$5 \times 10^5$</td>
<td></td>
</tr>
<tr>
<td>Single pe signal</td>
<td>80 fc</td>
<td></td>
</tr>
<tr>
<td>Source capacitance</td>
<td>&lt; 20 pf</td>
<td></td>
</tr>
<tr>
<td>Input impedance</td>
<td>&lt; 200Ω</td>
<td></td>
</tr>
<tr>
<td>Shaping</td>
<td>Unipolar (RC-CR)</td>
<td></td>
</tr>
<tr>
<td>Peaking time</td>
<td>50 ns</td>
<td></td>
</tr>
<tr>
<td>Single pe signal at comparator</td>
<td>500 mv</td>
<td></td>
</tr>
<tr>
<td>Charge gain at comparator</td>
<td>6.25 mv/fc</td>
<td></td>
</tr>
<tr>
<td>Equivalent noise charge</td>
<td>&lt; 10% pe</td>
<td></td>
</tr>
<tr>
<td>Programmable threshold setting</td>
<td>0 – 1 pe</td>
<td>0 – 500 mv</td>
</tr>
<tr>
<td>System clock</td>
<td>40 MHz</td>
<td></td>
</tr>
</tbody>
</table>

2. Front End Topology

The front end will consist of three gain/shaper stages followed by a relatively fast comparator with differential outputs as shown in Figure 1.
The first two gain stages use single ended opamps with RC feedback. These provide the first two stages of gain and implement the unipolar shaping function. The final gain stage consists of a differential opamp to provide the required gain at the comparator input. In this way, the comparator input sees a fully differential signal at its input and output.

The differential signal will be presented to the comparator through a pair of resistors. There will be a differential output current DAC also attached to the comparator input nodes. The current supplied by the DAC will develop a differential DC voltage across the input resistors and thus constitutes the threshold voltage. Each channel will have its own DAC for a one-per-pixel threshold setting.

The peaking time of 50 ns was chosen so that, with threshold settings of order 0.5 pe or less, the pulse duration will exceed the clock period. Thus the discriminated pulses can be registered at the FPGA inputs with no loss due to narrow pulses. Alternatively, the FPGA can implement an edge triggered mode so that pulses will always be recorded even if they are much narrower than the clock period.

The Front End Board (FEB) will contain 32 independent integrator/shaper/comparator channels which will be connected to input pins on the FPGA.

### 3. System Topology

All Front End Boards will be identical. Each will have a USB port and two RJ45 connectors. The USB ports are used for communication with the host computer while the RJ45s will be used for “lateral” connections (via cat 5 cable jumpers) from one FEB to the next one “up” in the chain as shown in Figure 2.
Figure 2

The “bottom” board in the chain is designated as a Master. While all boards have their own (40 MHz) system clock crystal, for synchronicity the Master must transmit its system clock laterally “up” the chain to the next board. Each slave must in turn do likewise so that the whole chain is running on the system clock of the master and thus remains in synch.

The remaining lines in the cat5 jumper cables can be configured in a variety of ways determined by FPGA firmware. It is intended that, at the least, they function as a means of synchronizing the slave boards so that all time-stamp counters roll over in a predictable manner. For this purpose, only a SysClk (System Clock) and a SYNC pulse be defined.

Additional use of this lateral bus will be suggested later.

3.1. Addressing

By definition, the Master will be designated as Board Address 0. A four (or more) bit jumper field will be provided on all boards so that they can be uniquely addressed. In principle, though, this should not be necessary. Firmware can be designed so that the Master is automatically considered
board 0 even without the address jumpers, the next slave Address 1, and so on up the chain.

### 3.2. Data flow

As stated before, all FEBs have their own USB port and these can all be connected, through a USB hub, to the host computer. All hit data can be placed on the USB fifo of that board for off-loading by the host.

In principle, data volume of this detector is so small that it can easily be carried by a single USB port. The topology of Fig 1 allows for this possibility. This could be done by utilizing the lateral cat5 connections as local data buses. In this case, the Master would continually pull data from the slaves and present it on its own USB fifo. Thus, only one USB port would be used for the entire Master/Slave chain.

### 3.3. USB Interface

USB interfacing will make use of a Cypress USB interface device, the CY7C68013A. There will be an associated memory connected to this chip to retain the chip’s “configuration”. Access to this prom will be through the USB interface itself. Cypress provides all the utilities necessary to do this configuration. It has been our experience that when used with the Cypress provided driver (dll), the interface achieves in excess of 100 Mb/s which is orders of magnitude greater than required for this application.

### 3.4. FPGA including configuration

A Xilinx FPGA will be chosen based on the firmware requirements of the design. These requirements should be transmitted to us in order to estimate the size and resources of the FPGA chosen. Alternatively, UT can simply choose the device for us to use. We will place a serial prom on the board and a standard JTAG connector through which it is programmed. A standard Xilinx JTAG download cable will be required by UT. FEB firmware can be field replaced by via this cable.

### 3.5. Lateral (Cat 5) Network Cable

The following describes the minimum functionality of the Lateral Network Cable as well as optional uses as determined by FPGA firmware.

#### 3.5.1. Minimum functionality

- The system clock (40 MHz) which is driven from the Master and is utilized by all Slaves “above” it in the chain for their own
system clock. FPGA firmware can be designed so that any board will function as a Master or Slave. If the board senses a Clock from “below” it assumes it’s a Slave and uses that clock. If not, it assumes it’s a master.

- A Sync signal sent from the Master upwards to all the Slaves. This serves to synchronize all real time clock counters in the system.

3.5.2. Optional functionality

This refers to the lateral Master/Slave communication port as mentioned above.

In the case of NOvA, FEBs are arranged in a “star”, not a daisy chain, but the system “controller” does implement a local protocol on a Cat 5 cable to all the FEBs. Timing, SYNC, command, and data are all transmitted via this bus. In the NOvA case, a semi-custom 8b/10b protocol is used. In the case of the NPD, it’s likely that a much simpler choice would suffice although the NOvA 8b/10b is rather straightforward and quite suitable.

If there is interest in this option, we could look into other protocol choices and report on them at a later time.